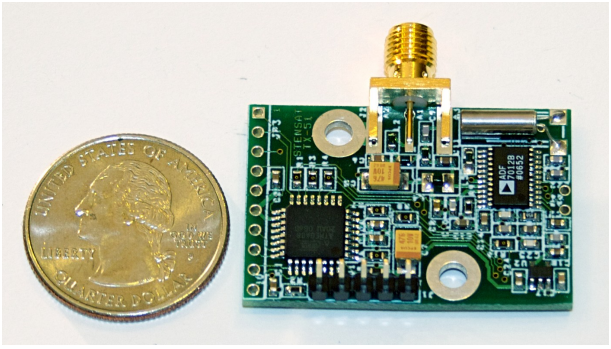
Stensat Transmitter Module

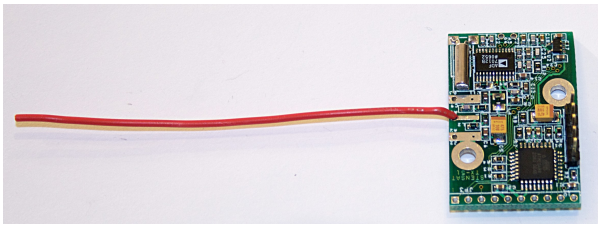
Stensat Group LLC

Introduction

The Stensat Transmitter Module is an RF subsystem designed for applications where a low-cost low-power radio link is required. The Transmitter Module is compatible with the AX.25 protocol using Unnumbered Information (UI) packets, and is capable of operating at 1200 bps and 9600 bps. The data packets can be formatted to conform to the APRS packet structure.



Transmitter with SMA option

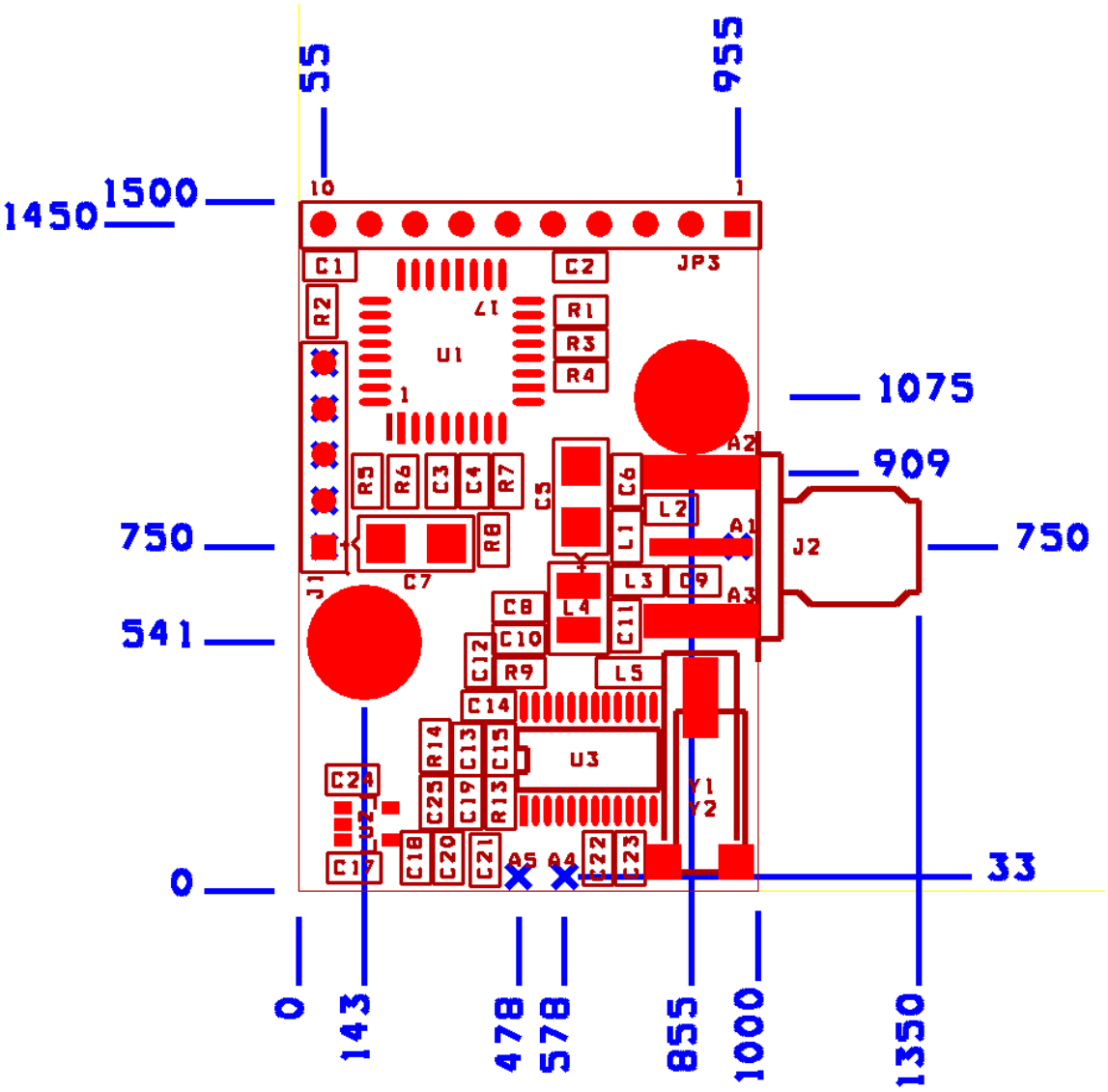


Transmitter With Wire Antenna

Specifications

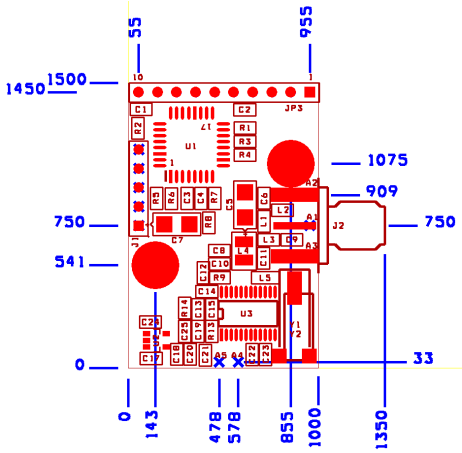
Item	Value
Bands available	2m, 70cm, 33cm
RF Output Power	+6 to +10 dBm
Operating voltage (Vdd)	3.3 to 5.0 volts
Operating Current	45ma when transmitting 12ma when idle
Serial Interface rate	38.4Kbaud
Dimensions	1.00” x 1.50” x 0.50” without SMA connector 1.35” x 1.50” x 0.50” with SMA connector
Mass	approx. TBD g
Digital Input signal specifications	High signal > 0.7*Vdd Low signal < 0.3*Vdd, 10 uA
Digital Output signal specifications	High signal > 2.0 volts Low signal < 0.4 volts, 3 ma sink
Mounting Holes	.125 inches, 4-40 mounting hardware
Frequency Ranges	
STM-51-01	902-928 MHz
STM-51-02	420-450 MHz
STM-51-03	144-148 MHz

Dimension Drawing

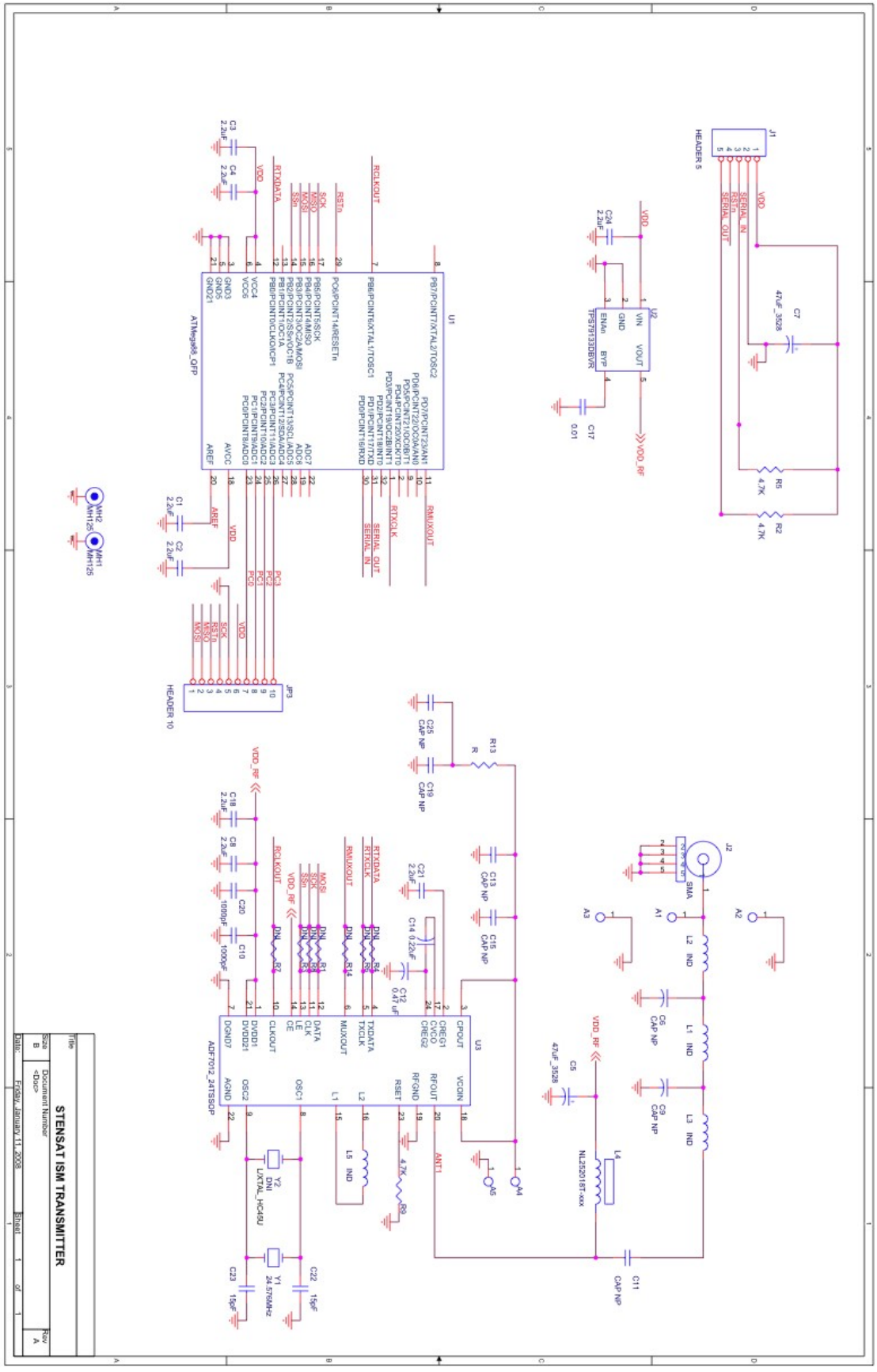


(units are 1/1000 inch)

Actual size:



Schematic


HEADER 5
J1
VDD
SERIAL_IN
RSTn
SERIAL_OUT
C7
47uF_3528
R5
4.7K
R2
4.7K
C24
2.2uF
VIN
GND
ENAn
BYP
VOUT
TPS79133DBVR
C17
0.01
VDD_RF
SMA
J2
A1
A2
A3
L2
IND
L1
IND
L3
IND
C6
CAP NP
C9
CAP NP
C5
47uF_3528
L4
NL252018T-xxx
C11
CAP NP
ANT1
U1
ATMega88_QFP
RCLKOUT
RSTn
SCK
MISO
MOSI
SSn
RTXDATA
RMUXOUT
RTXCLK
SERIAL_OUT
SERIAL_IN
C3
2.2uF
C4
2.2uF
C1
2.2uF
C2
2.2uF
MH2
MH125
MH1
MH125
JP3
HEADER 10
C25
CAP NP
C19
CAP NP
R13
R
C13
CAP NP
C15
CAP NP
C21
2.2uF
C14
0.22uF
C12
0.47 uF
U3
ADF7012_24TSSOP
CPOUT
VCOIN
CREG1
CVCO
CREG2
RFOUT
RFGND
RSET
TXDATA
TXCLK
MUXOUT
DATA
CLK
LE
CE
CLKOUT
DVDD1
DVDD21
DGND7
AGND
OSC2
OSC1
L1
L2
L5
IND
R9
4.7K
Y2
DNI
LiXTAL_HC49U
Y1
24.576MHz
C22
15pF
C23
15pF
C18
2.2uF
C8
2.2uF
C20
1000pF
C10
1000pF
R1
R2
R3
R4
R5
R6
R7
R8
R14
DNI
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STENSAT ISM TRANSMITTER
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Connection Information

5 Pin Header (J1)

Pin	Description
1	VDD, Positive supply, 3.3 to 5 volts
2	Ground
3	Serial Data In, 38.4Kbaud, 8 bit, no parity, one stop bit
4	Reset (active low)
5	Serial Data Out, 38.4Kbaud, 8 bit, no parity, one stop bit

10 Pin Header (JP3)

Pin	Description
1	MOSI, Digital IO or SPI Data output
2	MISO, Digital IO or SPI Data input
3	RST, reset (active low)
4	SCK, Digital IO or SPI clock
5	Ground
6	VDD, positive supply, 3.3 to 5 volts, same as pin1 on 5 pin header
7	PC0, Digital IO or ADC input 0
8	PC1, Digital IO or ADC input 1
9	PC2, Digital IO or ADC input 2
10	PC3, Digital IO or ADC input 3

Description

The transmitter module consists of two major integrated circuits - the Atmel ATMega88 AVR processor and the Analog Devices ADF7012 transmitter. The ATMega88 is an 8-bit RISC processor operating at 12.288 MHz. The processor has 8 Kbytes of program memory and 1KByte of Data memory.

The ADF7012 includes a synthesizer, a VCO, and modulation circuitry to support different modulations including FSK, GFSK, and OOK. Four registers can be programmed to set the operating frequency. External components set the frequency band and phase lock loop filter characteristics. Components are installed at the factory for each operating band.

The software provided with the Stensat Transmitter Module provides a simple mechanism for sending data. User data is provided in a Command-plus-Data format, and the Transmitter Module performs the necessary formatting to meet the AX.25 requirements.

Command Set

Command	Description	Format
C	Set source Call sign	Ccccccc<CR>
D	Set Destination call sign	Ddddddd<CR>
V	Set Via (relay) call sign	Vvvvvvv<CR>
S	Send ASCII String	Sssssssssss…sssss<CR>
F	Set the Frequency	Fffff<CR>
M	Set the bit-rate Mode	M1200<CR> or M9600<CR>

All commands are ASCII sequences terminated with a carriage return character (<CR>; hex 0x0D; decimal 013.) Line Feeds (<LF>; hex 0x0A; decimal 010.) are discarded. The first character of the sequence is the Command character identified in the table above, and is always capitalized (the commands are case-sensitive.) Immediately following the Command is the user data parameter. The command is terminated with a <CR>. Individual bytes are sent to the Transmitter Module in the desired order of transmission, beginning with the byte immediately following the Command character.

Call signs can be no larger than six characters, but may be less than six characters. If fewer than six characters are provided, the Transmitter Module will add trailing spaces to the six-character call sign per the AX.25 specification. The Transmitter Module does not check for valid call sign formats and will transmit whatever is entered. Some TNCs will not decode packets with malformed call signs.

The three call sign parameters have the following power-up default values:

Source - CANSAT
Destination - CQ
Via - TELEM

When sending an ASCII string, only ASCII characters are valid as data. Control codes will confuse some TNCs. Up to 200 characters can be transmitted in one packet. Transmission of the AX.25 packet starts immediately upon detection of the carriage return. During the RF transmission period, the Transmitter Module will disregard inputs on the serial command interface.

Setting the frequency requires a detailed understanding of how the synthesizer generates the RF frequencies. A table of values is available on the Stensat website to help in selecting frequencies.

The baud rate Mode command allows selection of either 1200 bps AFSK or 9600 bps FSK. Mode changes may be made at any time, and become effective immediately.

Example C Code

This example is used to show how the commands are formatted. Actual methods to perform serial communications will vary depending on the host system implementation.

```
#include <stdio.h>

int number;                    // example variable
char cmd[200];                 // command array to send to transmitter

main()
{
        sprintf(cmd,"CKM4JDG\r");          // set source call sign to KM4JDG
        send_serial(cmd);

        send_serial("M9600\r");            // set the operating mode to 9600bps FSK
        number = 5;
        sprintf(cmd,"Sthis is a test of the data packet transmission number %d\r",number);
        send_serial(cmd);                  // send the above string
}
```

Advanced Topics

This section provides a low-level description of the hardware implementation. **Please note that it is possible to "brick" the Transmitter through improper programming procedures.**

ATMega88 Programming

The ATMega88 programming pins are available on the first six pins of the JP3 header. Four signals plus power and ground are required for programming. An appropriate cable adapter will be necessary to interface your AVR programmer to the Transmitter Module. *Stensat Group does not supply any AVR programming hardware (nor do we supply technical support of programming hardware.)*

The processor clock is generated by the ADF7012. The ADF7012 configuration data port uses the same SPI signals as the programmer. The programming sequence may be interpreted by the ADF7012 as a legitimate configuration word. It is possible to disable the clock output to the ATMega88. A lack of clock will cause the ATMega88 to stop functioning. Recovering the Transmitter Module from a "no clock" configuration requires factory intervention. **It is advised that the following programming procedure be used:**

- **Change the ATMega88 clock configuration to "internal RC oscillator"**
- **Program the Atmega88**
- **Revert the ATMega88 clock configuration to "external clock"**

The ATMega88 requires a valid clock source during the programming phase. Changing to the Internal RC clock will guarantee that a valid clock is available. The RC clock is not precise enough for serial baud rate generation, and thus is not used during normal operation.

The 10-pin header used for programming the ATMega88 processor also carries four pins connected to the ATMega88 port pins C0-C3. These ports can be configured as digital I/O or as inputs to the ATMega88's 10-bit analog-to-digital converter (ADC). The signals on the 10-pin header can be used to interface to other devices. These pins are un-allocated in the default factory software load.

Configuring the ADF7012

The ATMega88 configures the ADF7012 through the SPI port. The ADF7012 is a write-only device, and does not support readback functions. I/O pin B2 of the ATMega88 is set low during the configuration sequence and raised when each register parameter has been written. Configuration registers within the ADF7012 set the operating range in conjunction with the external components. Please refer to the ADF7012 data sheet for detailed information about configuration values.

Modulation Output

The ATMega88 pin B0 drives the data modulation signal to the ADF7012. During 1200 bps AFSK packet mode, pin B0 toggles the ADF7012 between two RF frequencies at the specified audio tone rate - either 1200 or 2200 Hz. When operating at 9600 bps, the ADF7012 provides a carrier-synchronous clock RTXCLK signal to the ATMega88's Interrupt 1 input. The Atmega88 detects the transition of the RTXCLK signal and sends out the next packet data bit. RTXCLK operates at 9600 Hz. The ADF7012 is configured to use a gaussian filter with the packet data stream, which is compatible with 9600 baud TNCs.

Ordering Information

Part Number	Description
STM-51-01	Transmitter Module, 900 MHz (33cm) band, no SMA connector
STM-51-01-C	Transmitter Module, 900 MHz (33cm) band, SMA connector installed
STM-51-02	Transmitter Module, 430 MHz (70cm) band, no SMA connector
STM-51-02-C	Transmitter Module, 430 MHz (70cm) band, SMA connector installed
STM-51-03	Transmitter Module, 144 MHz (2m) band, no SMA connector
STM-51-03-C	Transmitter Module, 144 MHz (2m) band, SMA connector installed